

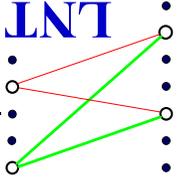
Recent Progress in Mobile Transmission

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St. Petersburg, Russia, April 6th, 2004

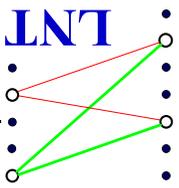


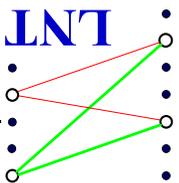
Outline

- The turbo principle approaches Shannon's limits
- MIMO systems allow high data rates in mobile systems
- Analog VLSI chips allow higher speed and low power consumption

Introduction

- **1948:** Shannon's absolute limits in communications, e.g. 0.2 dB in E_b/N_0 for binary codes with rate $1/2$ on AWGN channel
- **1962:** Gallager's low density parity check codes with iterative decoding
- **1966:** Forney: Concatenated codes
- **before 1993:** Concatenated codes (Viterbi plus RS codes) approach Shannon's limit by 2.5 dB and with iterations by 1.5 dB.
- **1993:** Berrou, Glavieux and Thitimajshima: Turbo decoding approaches Shannon's limit by 0.5 dB.
- **1995:** Douillard, Glavieux, Berrou et al: Turbo equalization
- **1997:** Turbo principle recognized as general method in communications systems
- **2001:** Chung, Forney, Richardson, Urbanke: Iterative decoding of Ir-regular LDPC Codes within 0.0045 dB of Shannon limit



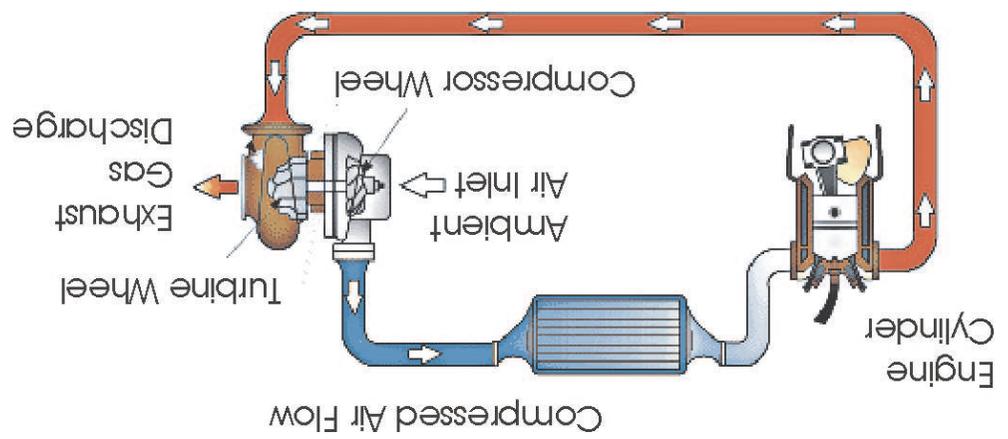


Introduction

The Turbo Principle comprises...

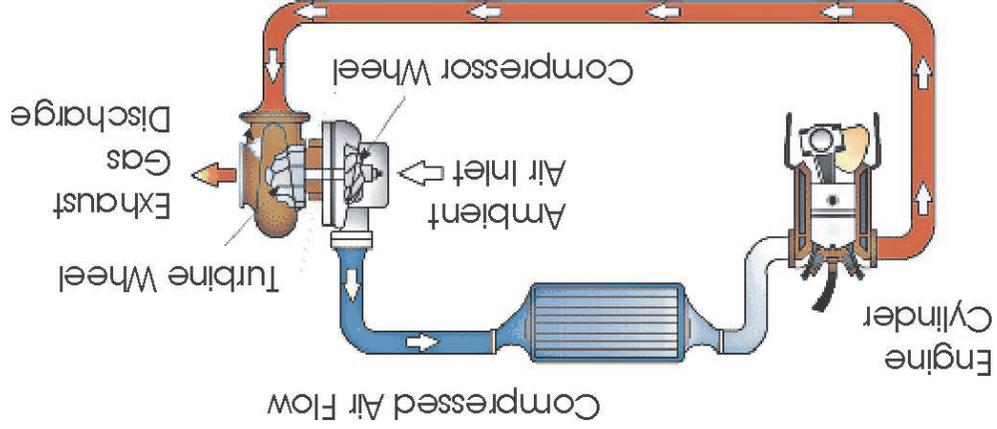
- ... a communication system with serial and/or parallel concatenations of components
- ... a posteriori probability (APP) symbol-by-symbol decoders/detectors
- ... soft-in/soft-out decoders/detectors
- ... interleavers between the components
- ... exchange of extrinsic information between components in the form of probabilities or log-likelihood ratios

The Turbo Principle ...



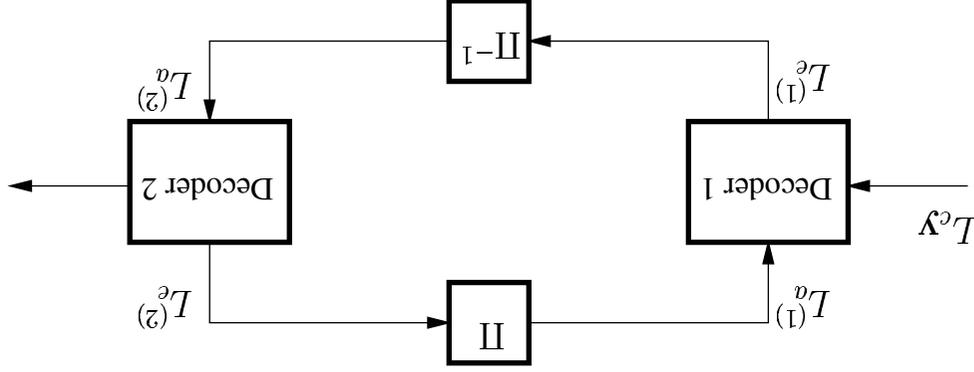
... in mechanics

... in mechanics

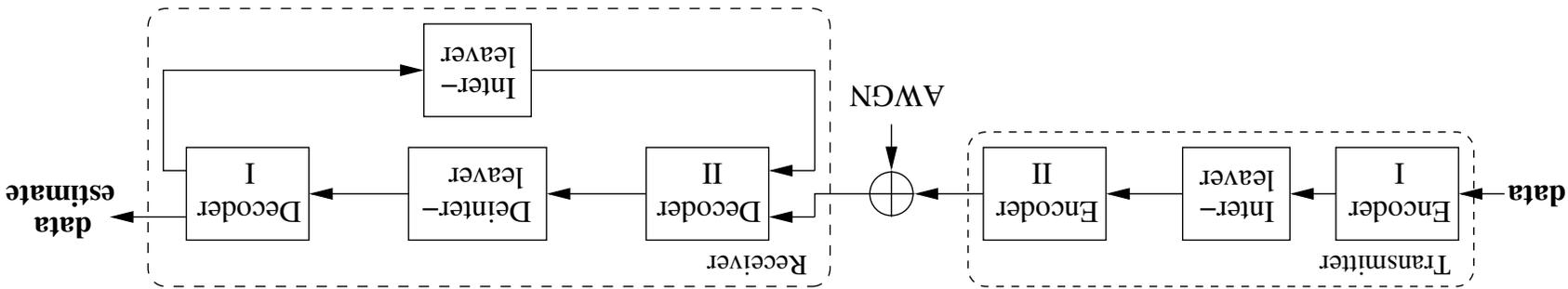


The Turbo Principle ...

... in communications



Examples for serial concatenation in communications systems

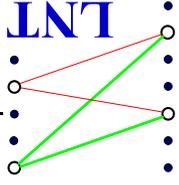
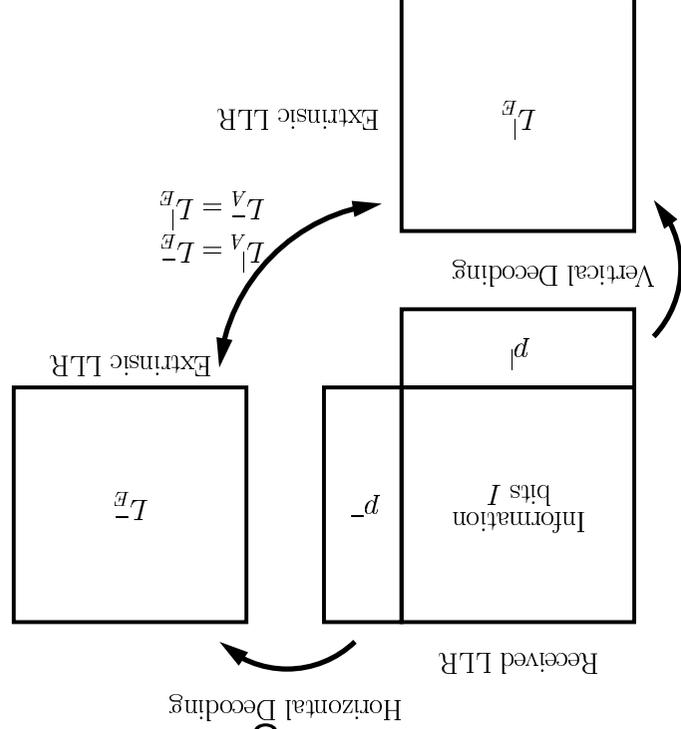


configuration	en-/decoder I (outer code)	en-/decoder II (inner code)
serial code concat.	FEC en-/decoder	FEC en-/decoder
turbo equalization	FEC en-/decoder	Multipath channel/detector
turbo BICM	FEC en-/decoder	Mapper/demapper
turbo MIMO	FEC en-/decoder	Mapper & MIMO detector
turbo multiuser	FEC en-/decoder	SISO multiuser detector
turbo source-channel	source encoder	FEC en-/decoder
LDPC code/decoder	check nodes	variable nodes

Principle of Turbo Decoding for a parallel concatenated scheme.

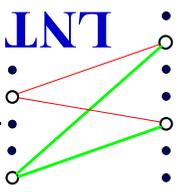
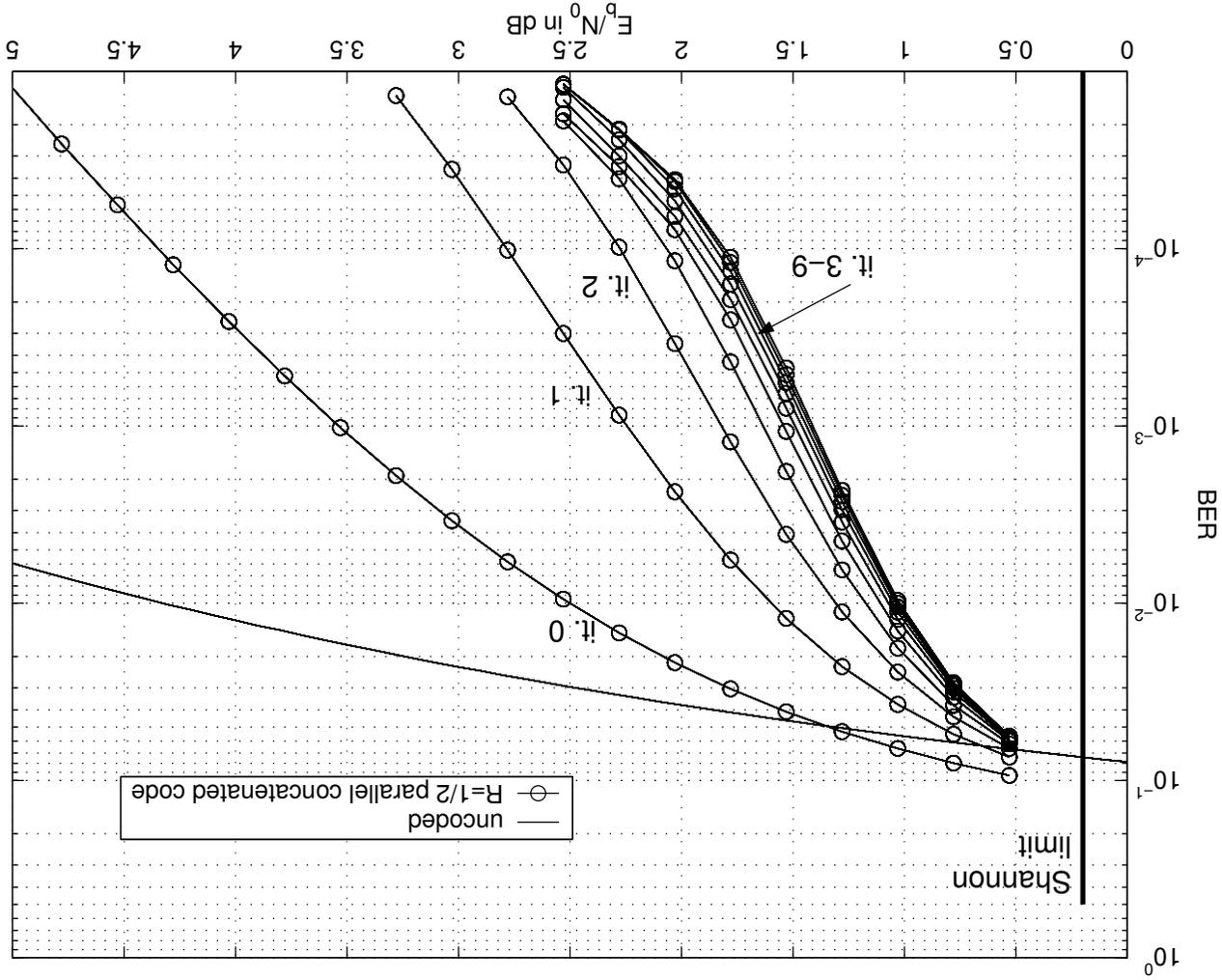
Exchange of **extrinsic** information between horizontal and vertical

decoding

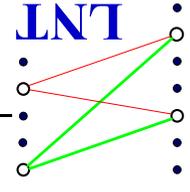
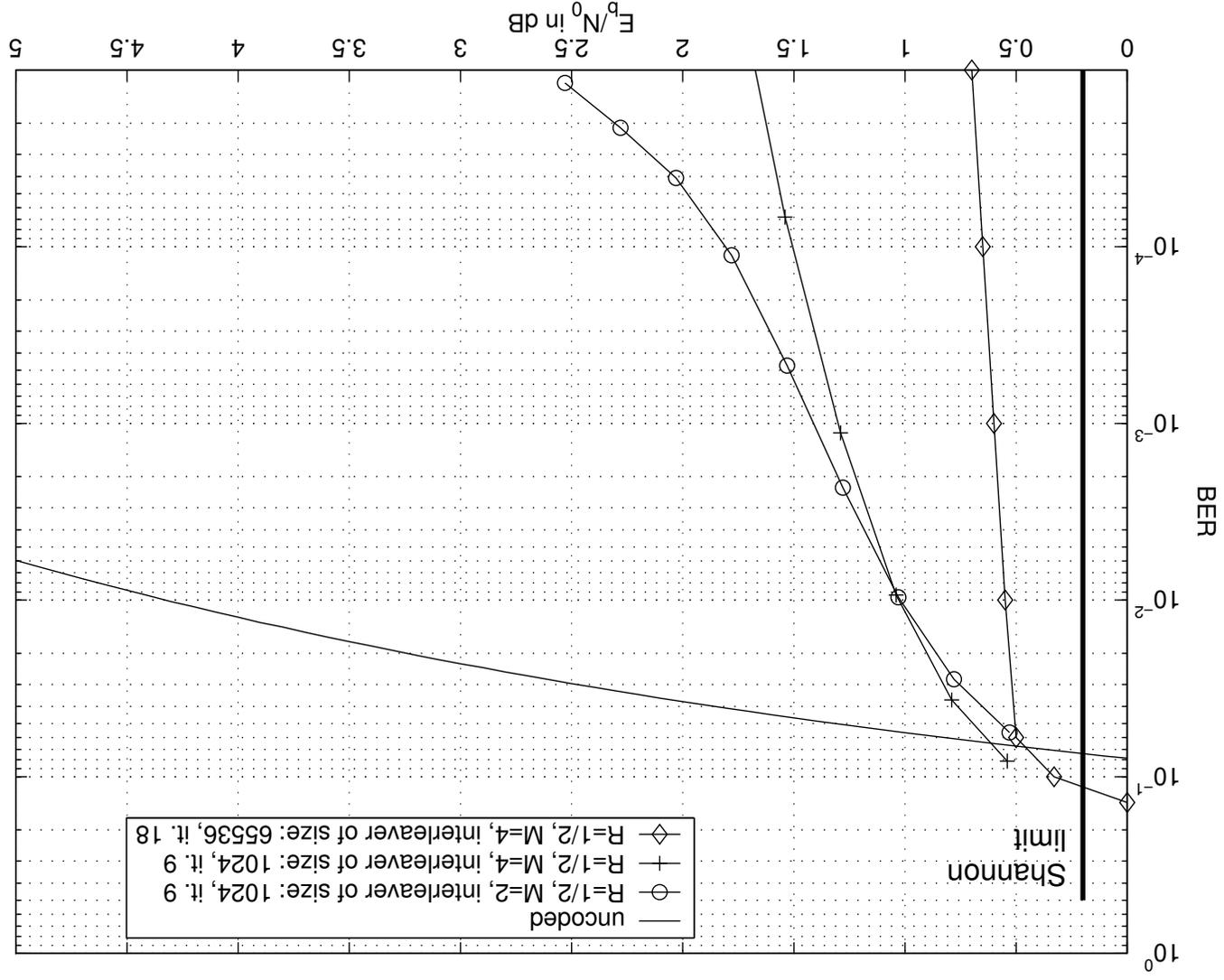


Performance of Decoder of a PCC Turbo Code

Rate 1/2, constituent code: rate 2/3, memory 2, interleaver size 1024

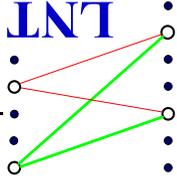
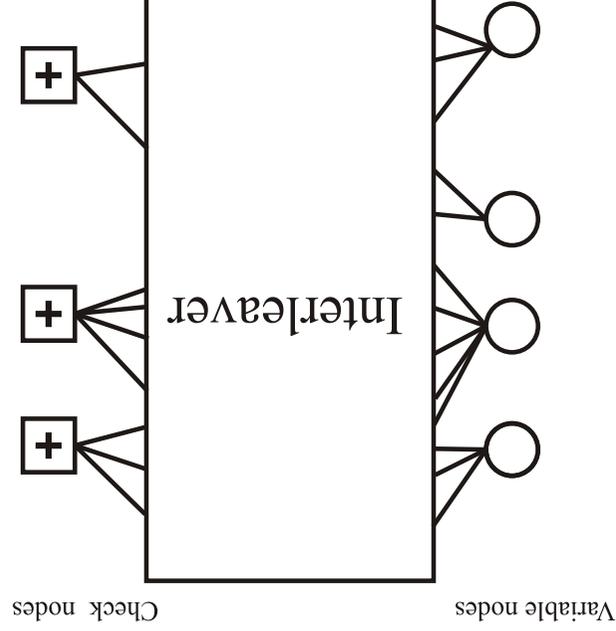


Influence of the Interleaver Size for a PCC Turbo Code

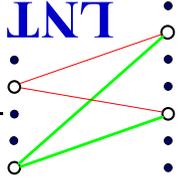
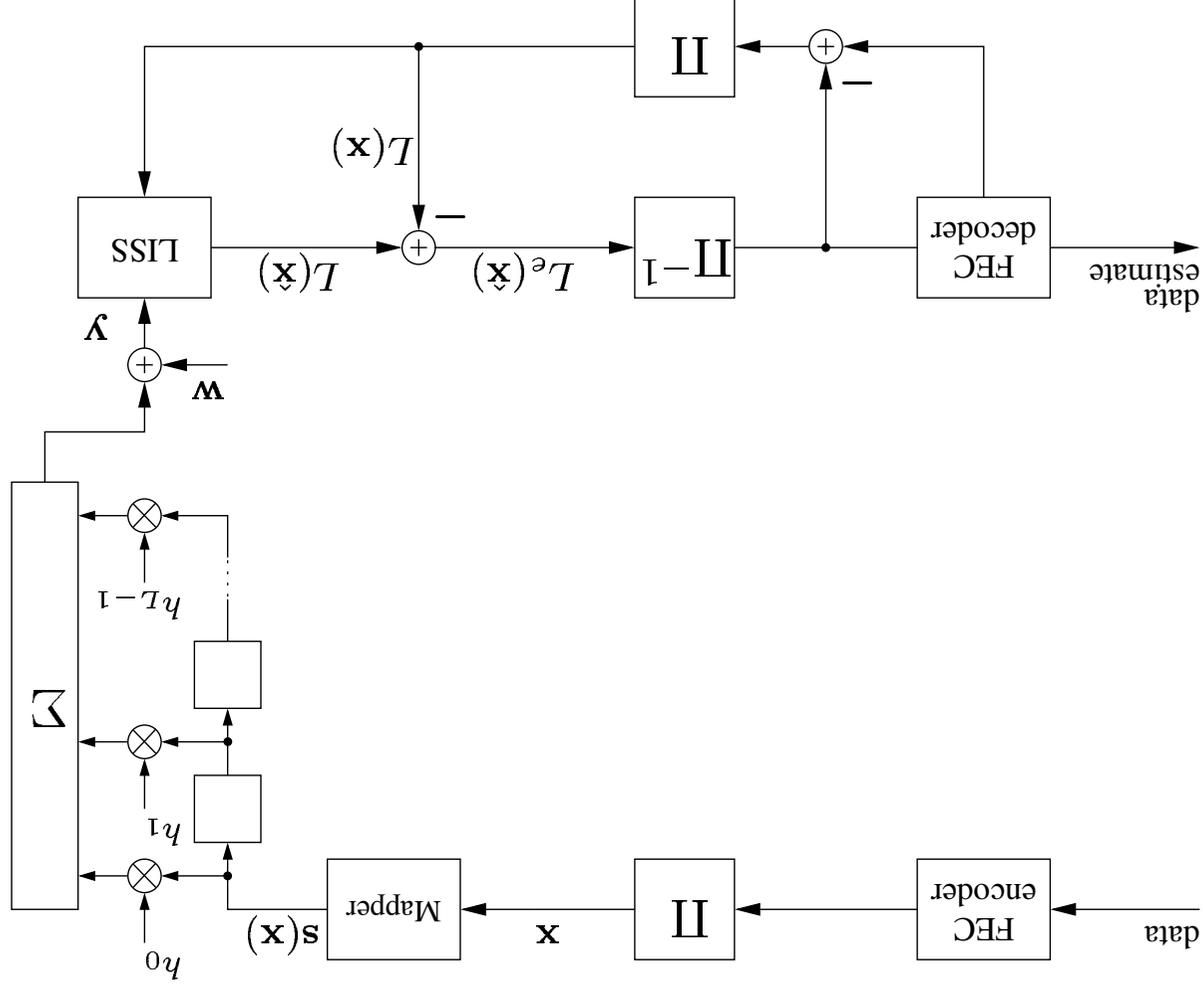


Low Density Parity Check (LDPC) codes and their Turbo decoder

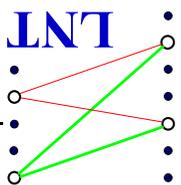
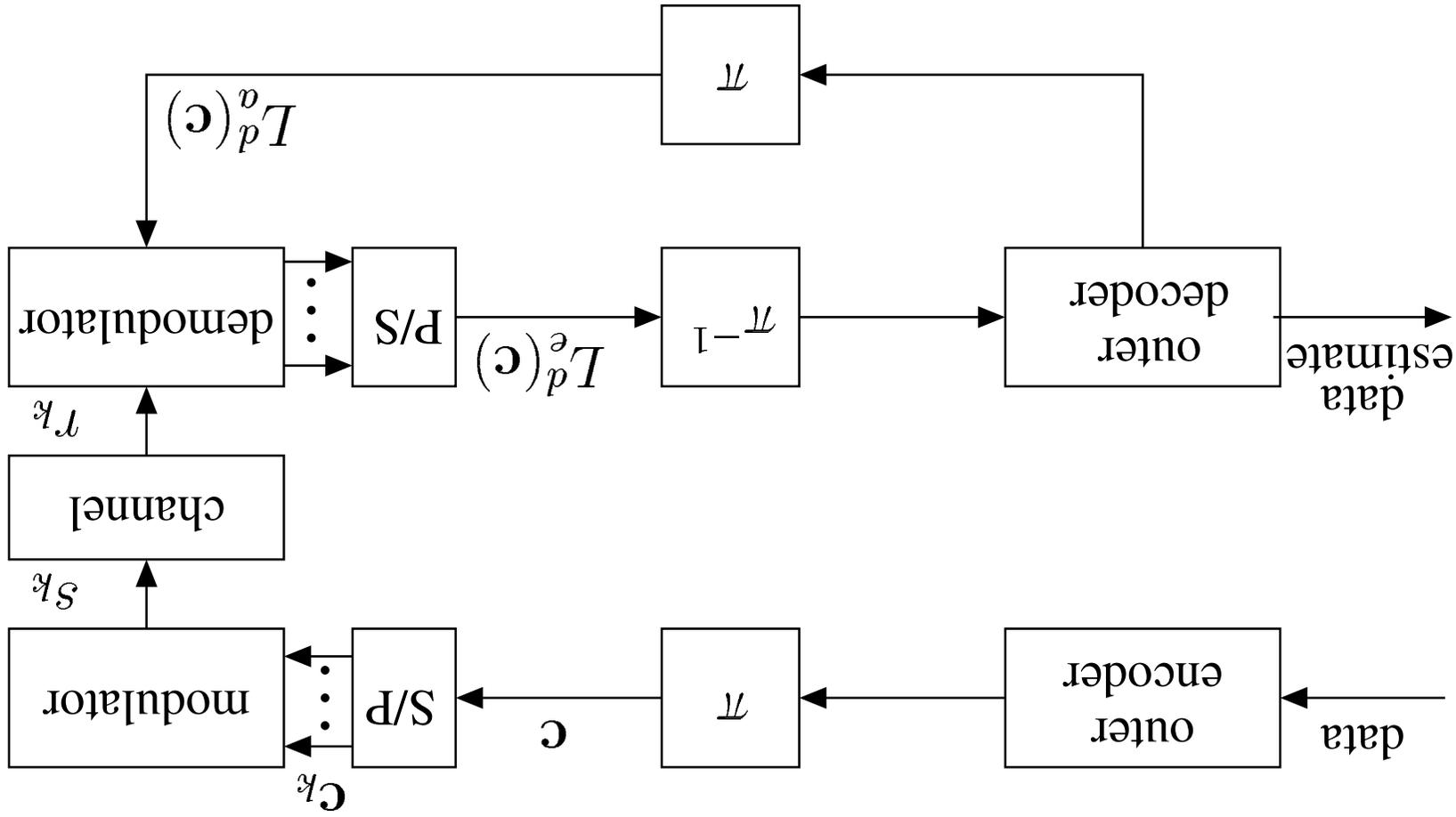
A low density parity check code of rate k/n can be described as a serial concatenation of n variable nodes as inner repetition codes with $n - k$ check nodes as outer single parity check nodes.



System with Multipath Channel and Receiver with Turbo Feedback



Turbo applications: QAM with channel codes

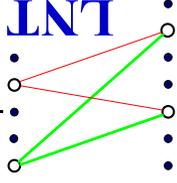


MIMO systems allow high data rates in mobile systems

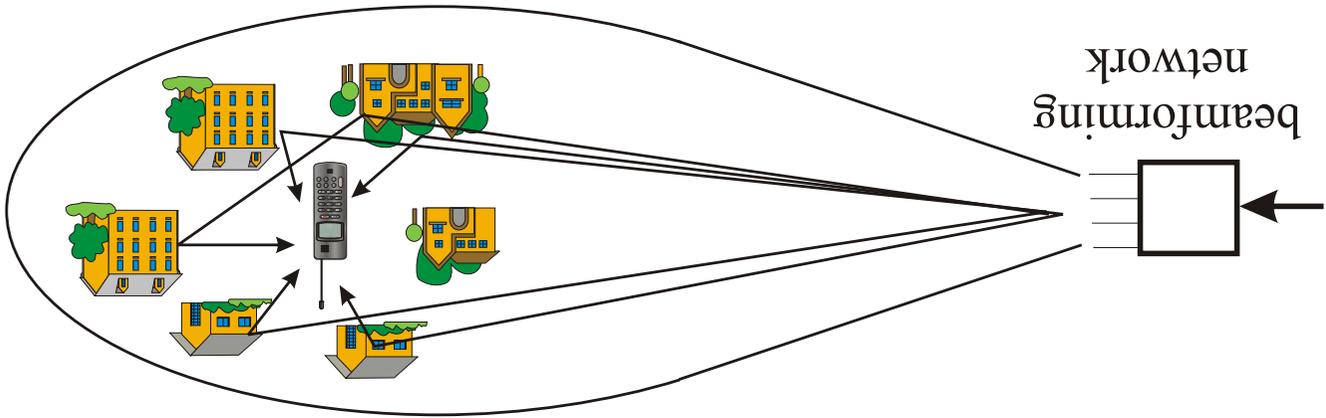
Classical Multiplex and Diversity Systems:

A new dimension is opened by space
(multiple transmit and receive antennas: MIMO)

Method	yields	costs
Time	Div. and rate gain	bandwidth
Frequency	Div. and rate gain	bandwidth
Code	Div. and rate gain	bandwidth, complexity and interference
Space	Div. and rate gain	complexity and interference

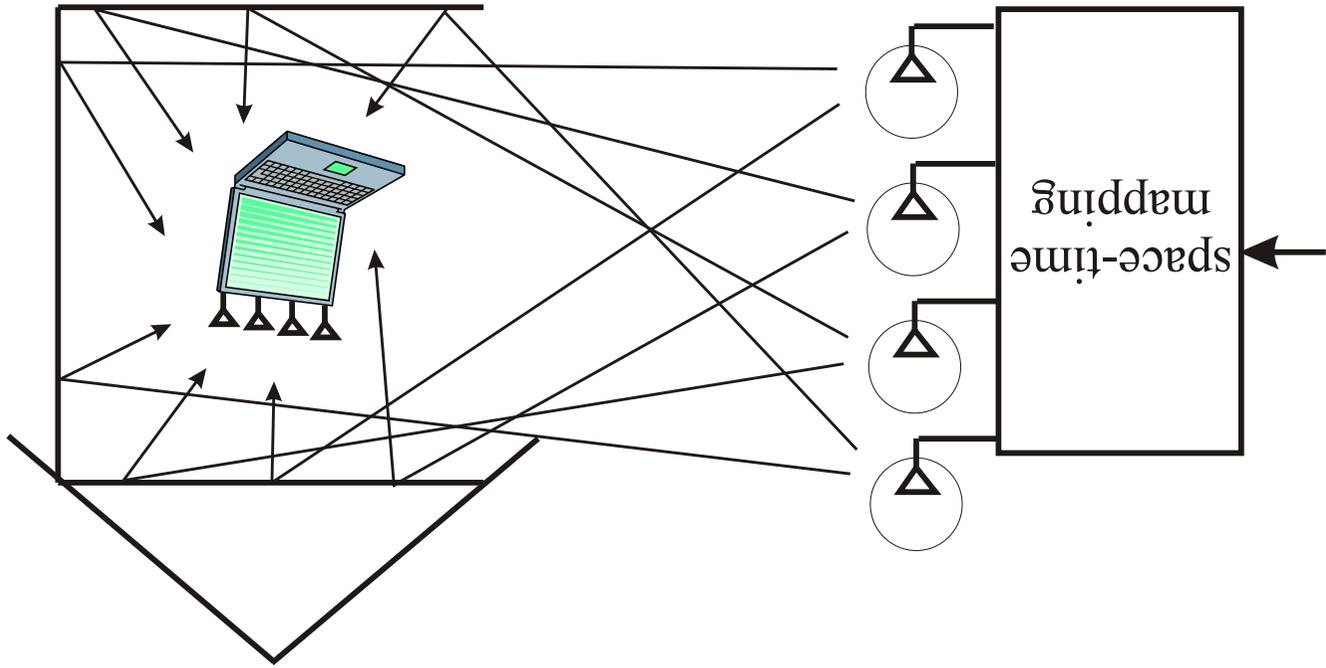


Beamforming antenna scenario



Beam can be made adaptive

Multiple antenna scenario aiming for rate gain

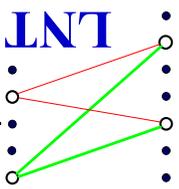
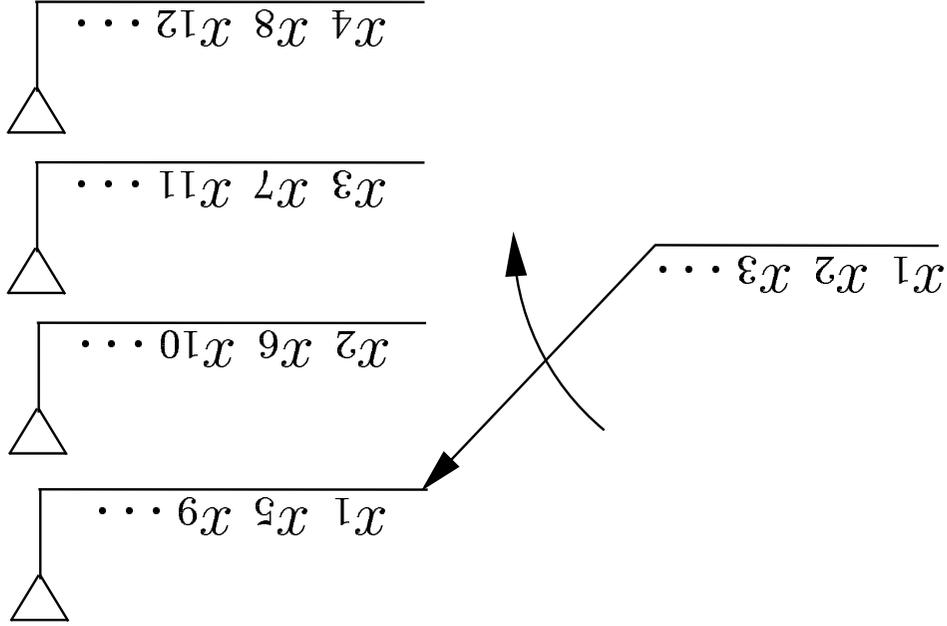


Multiple antennas needed at transmitter **and** receiver

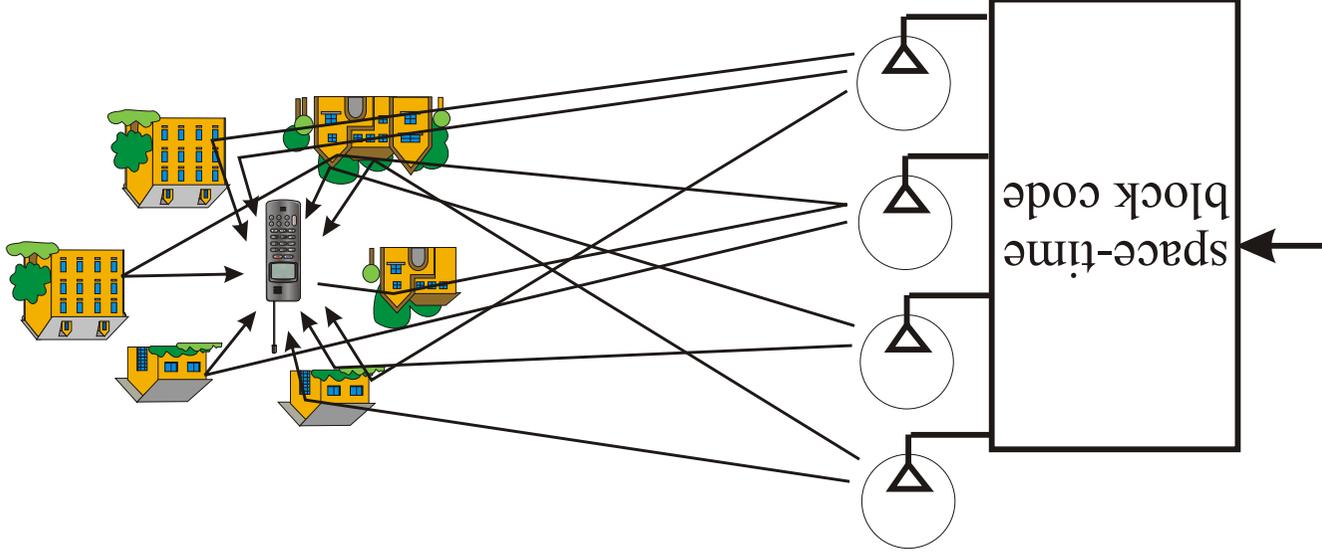
Systems aiming for rate gain

The Bell Lab Layered Space Time architecture (Foschini 1996 **BLAST**):

Example of V-BLAST for $N_T = 4$ and rate gain 4 if $N_R \geq 4$.

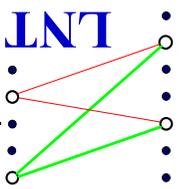


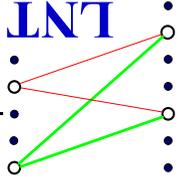
Multiple antenna scenario aiming for diversity gain



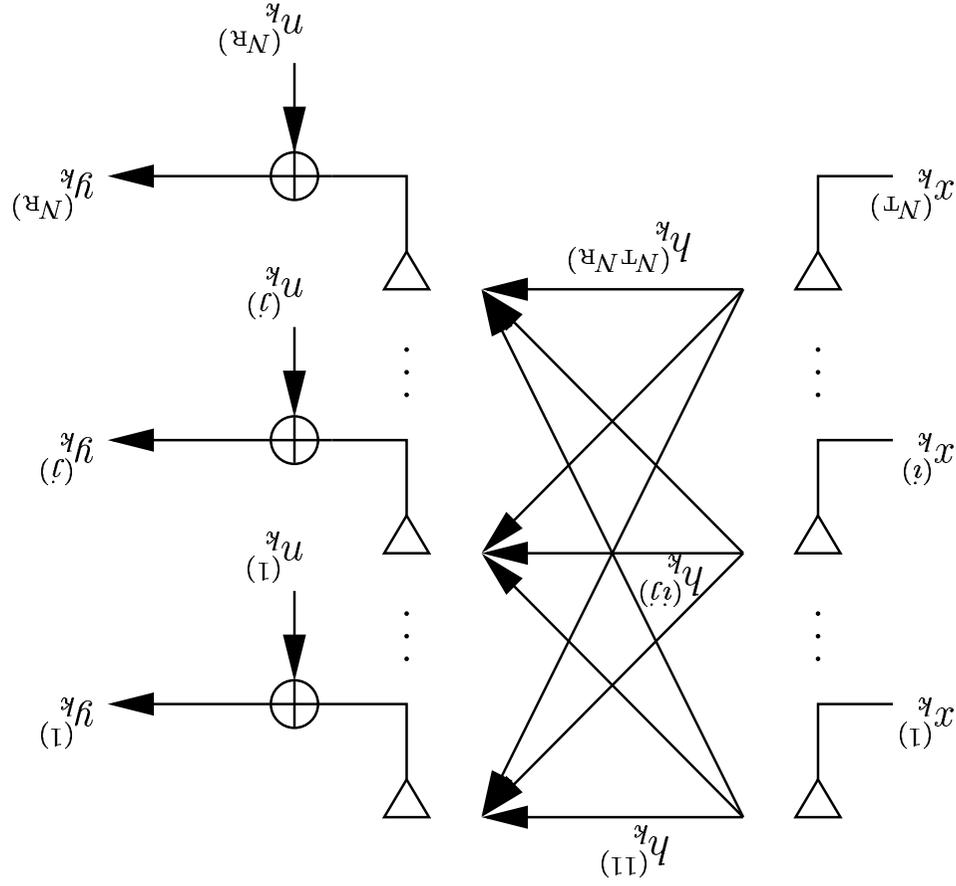
Transmit Diversity:

Receiver (i.e. cellphone) needs only **one and simple** antenna





$$\mathbf{y} = \mathbf{H}\mathbf{x} + \mathbf{n}$$



The multiple-antenna (MIMO) channel model

Channel capacities of SISO and MIMO systems (Telatar 1995)

The channel capacity for a single-input/single-output (SISO) fading channel with complex signaling and perfect channel knowledge at the receiver

$$C = \log_2(1 + |h_{(11)}|^2 \frac{E_s}{N_0})$$

and for the multiple-input/multiple-output MIMO channel

$$C = \log_2 \det \left[\mathbf{I}_{N_R} + \frac{E_s}{N_0} \mathbf{H} \mathbf{H}^H \right].$$

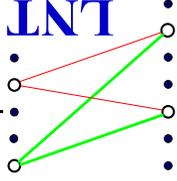
Both capacities measured in bits/channel use are random variables. Therefore the average (ergodic) capacity

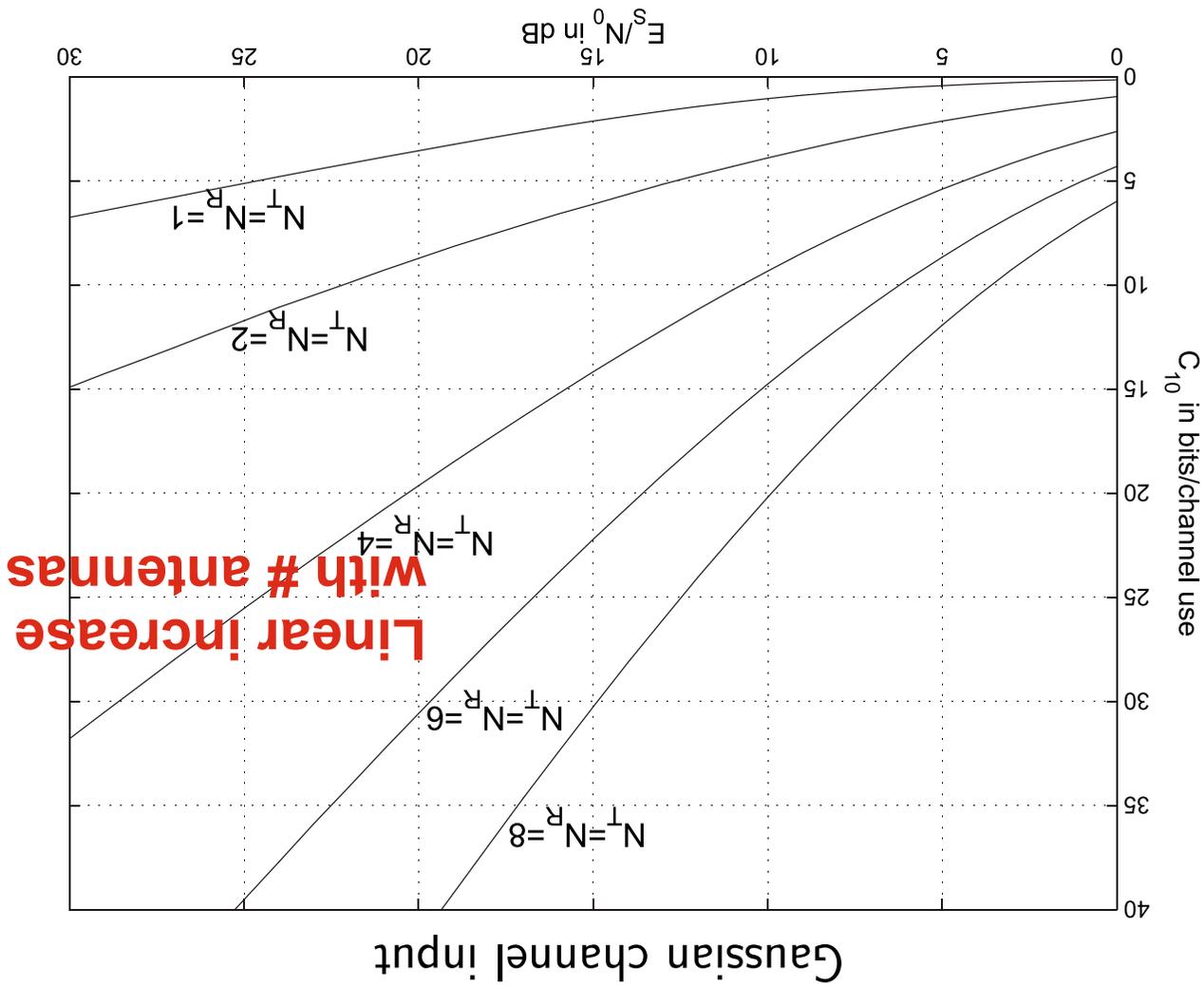
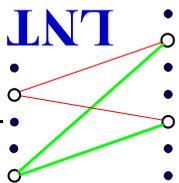
$$\bar{C} = E_H \{C\}$$

and the outage capacity

$$P(C > C_x) = \frac{x}{100}, \quad 0 < x < 100,$$

are of interest.



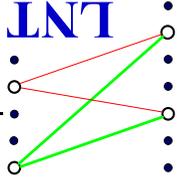
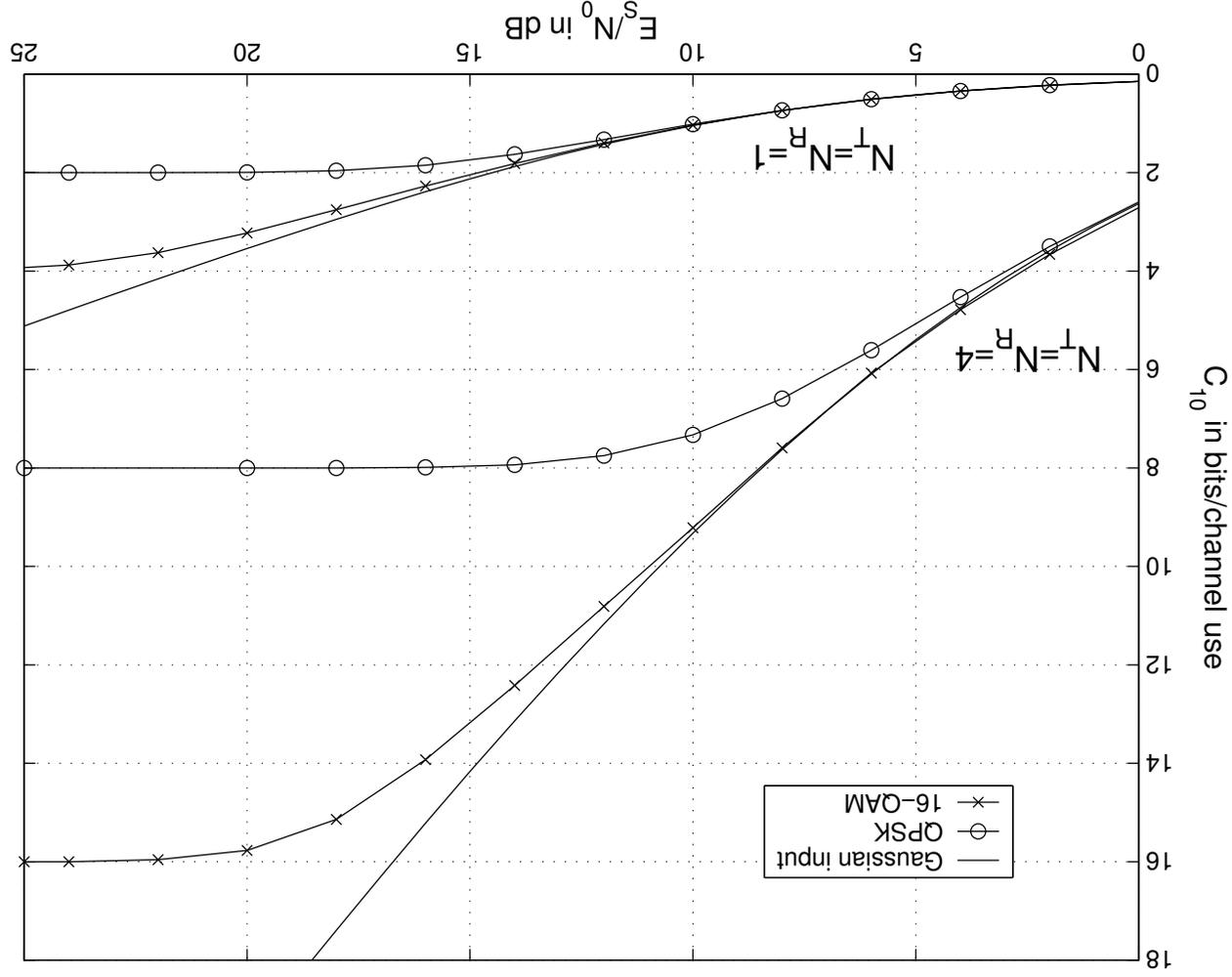


10% outage capacity of different MIMO channels

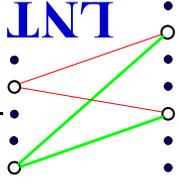
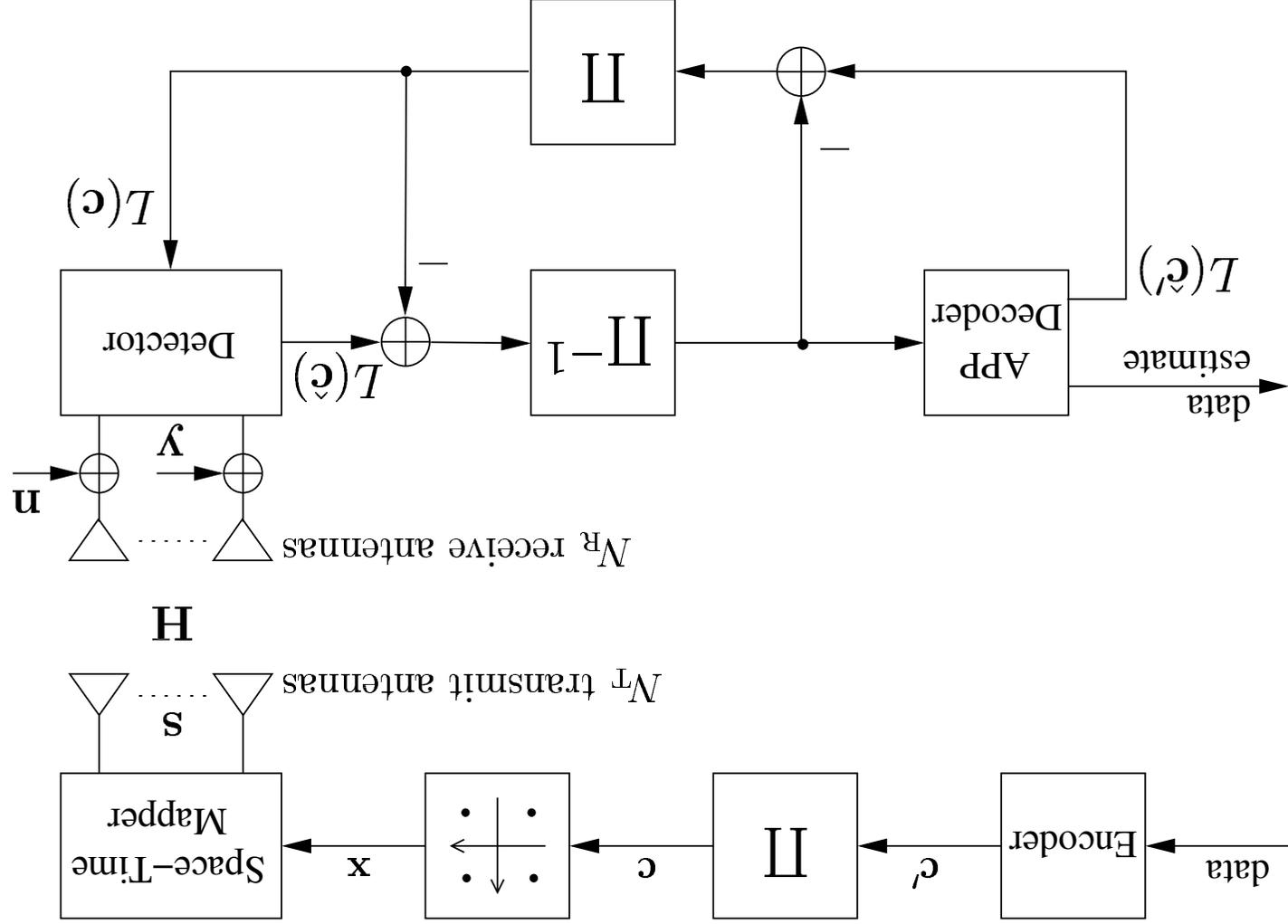
Linear increase
with # antennas

10% outage capacity of different MIMO channels

Discrete (QPSK, 16-QAM) and Gaussian channel input



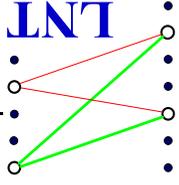
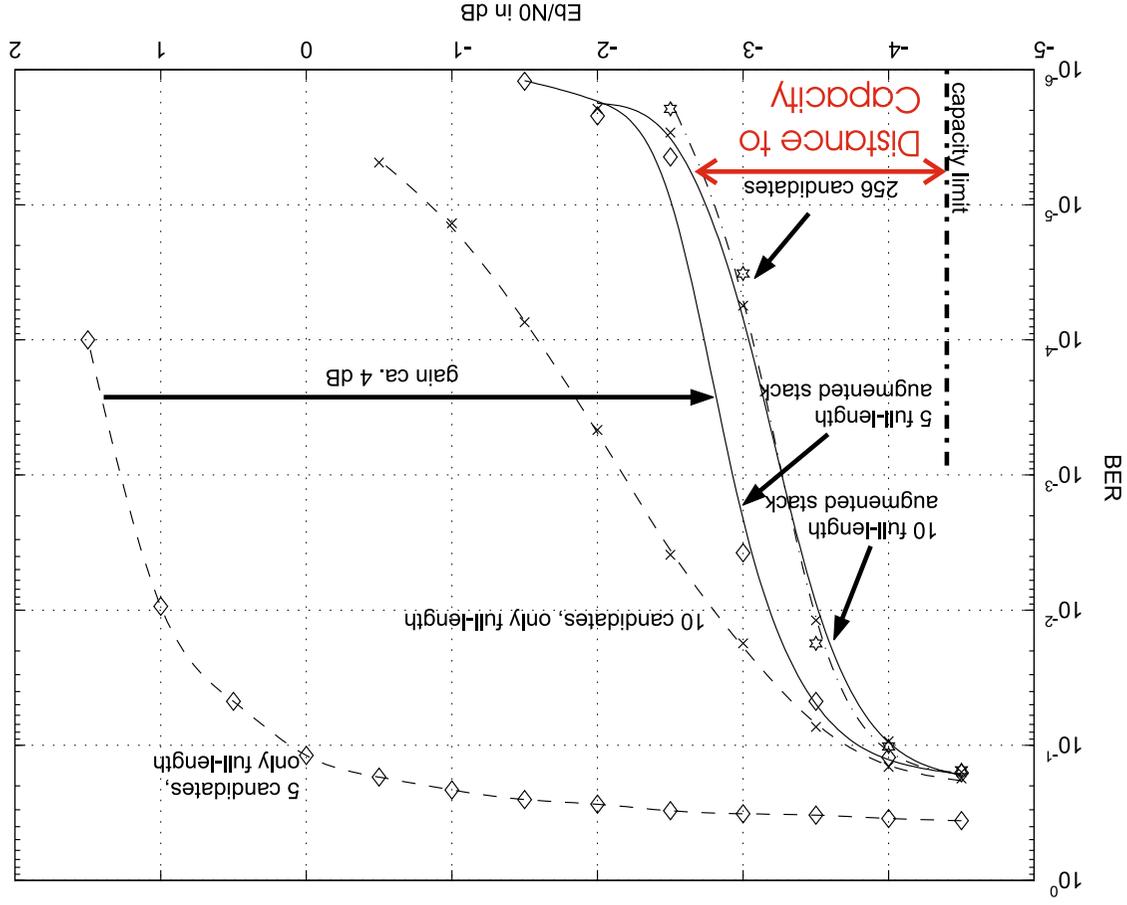
FEC-MIMO Scheme with Turbo detector/decoder

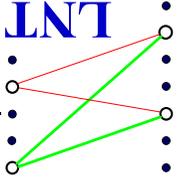


MIMO Turbo Detector

Inner MIMO channel with Sequential detector (LISS)

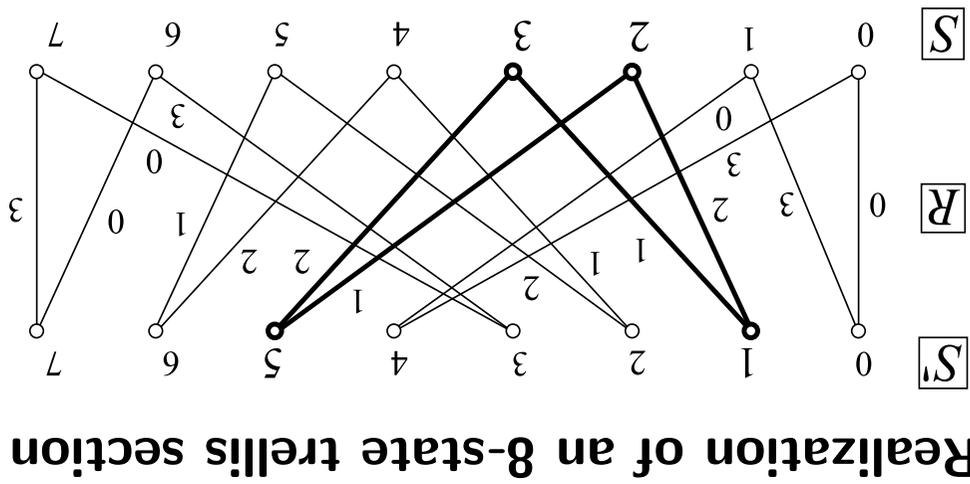
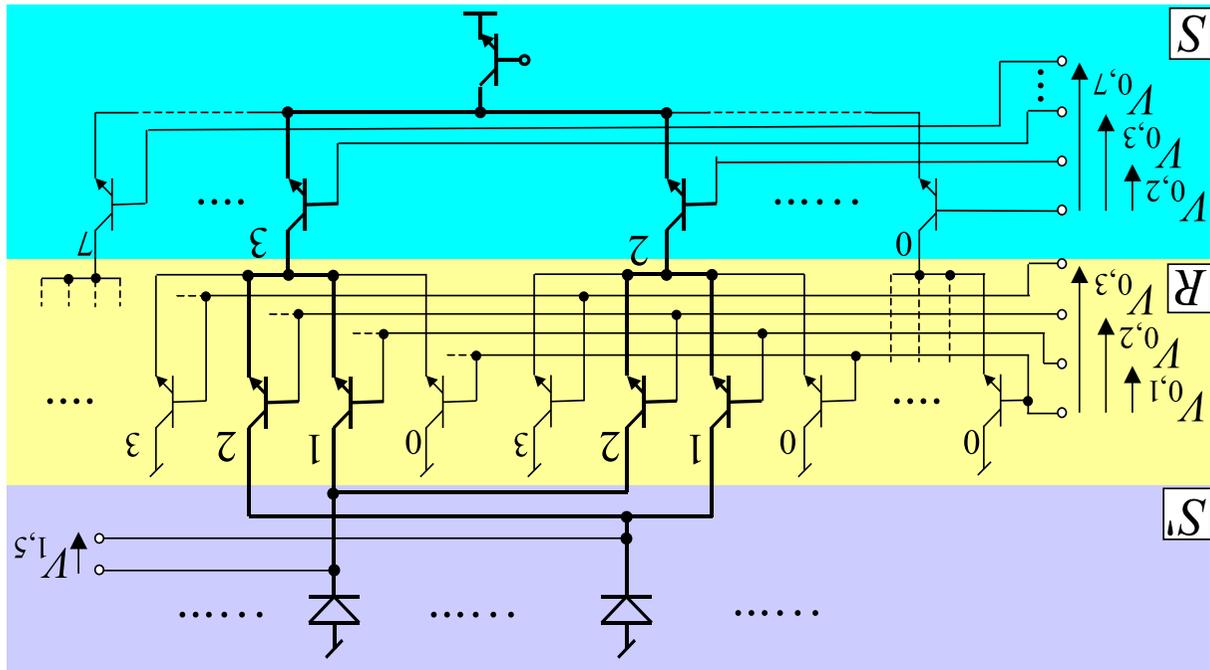
Simulation results: outer PCC code $r = 1/2$, QPSK, $N_T = N_R = 4$,

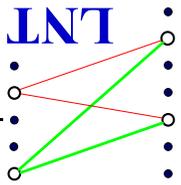




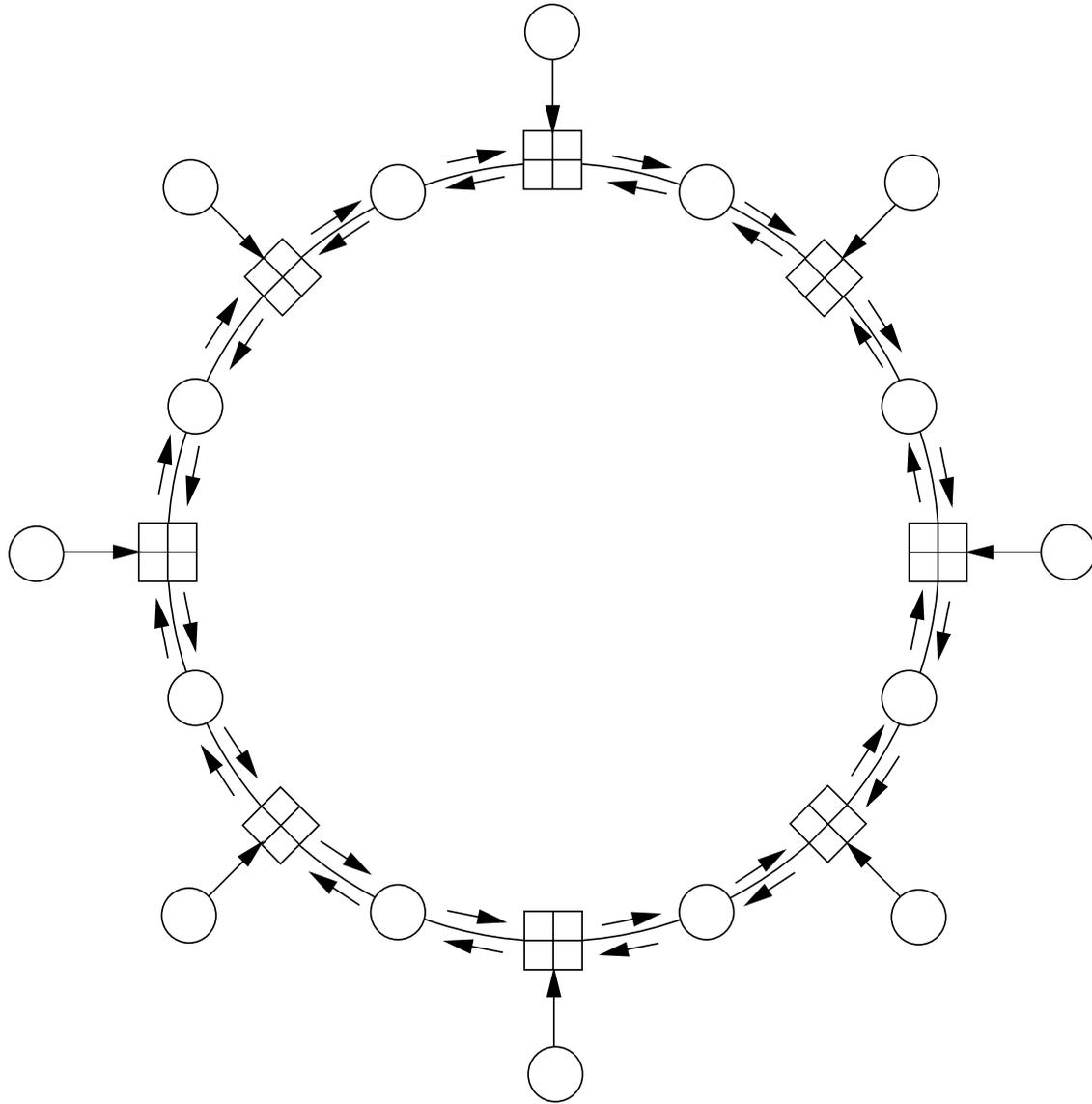
Introduction to analog decoders and receivers

- Receivers and decoders (especially turbo decoders) use soft (real and not binary) values (probabilities, log-likelihood values)
- They still operate in discrete time and with discrete operations
- Can we do decoding in continuous time and values: analog?
- Are receivers in analog VLSI possible?
- First Proposals: JH (ITW 98, ISIT 98), Loeliger (ISIT 98)
- High speed receivers in digital VLSI implementation are area and power consuming
- FEC decoders for high speed communications should work in the Gbit/s range
- Analog VLSI implementations of functions like Viterbi, APP, Turbo algorithm should be faster smaller and less power consuming



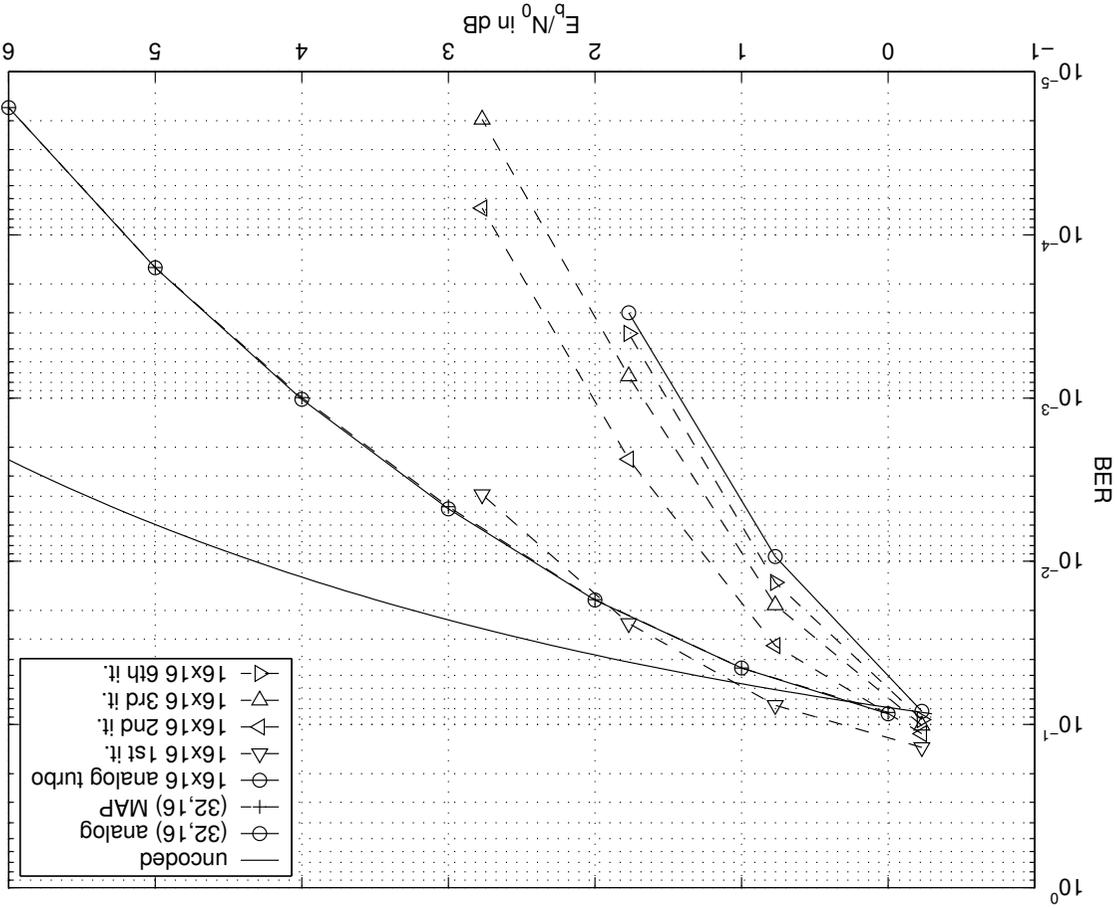


Memory one tailbiting convolutional code

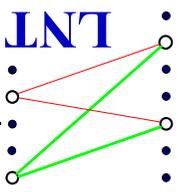


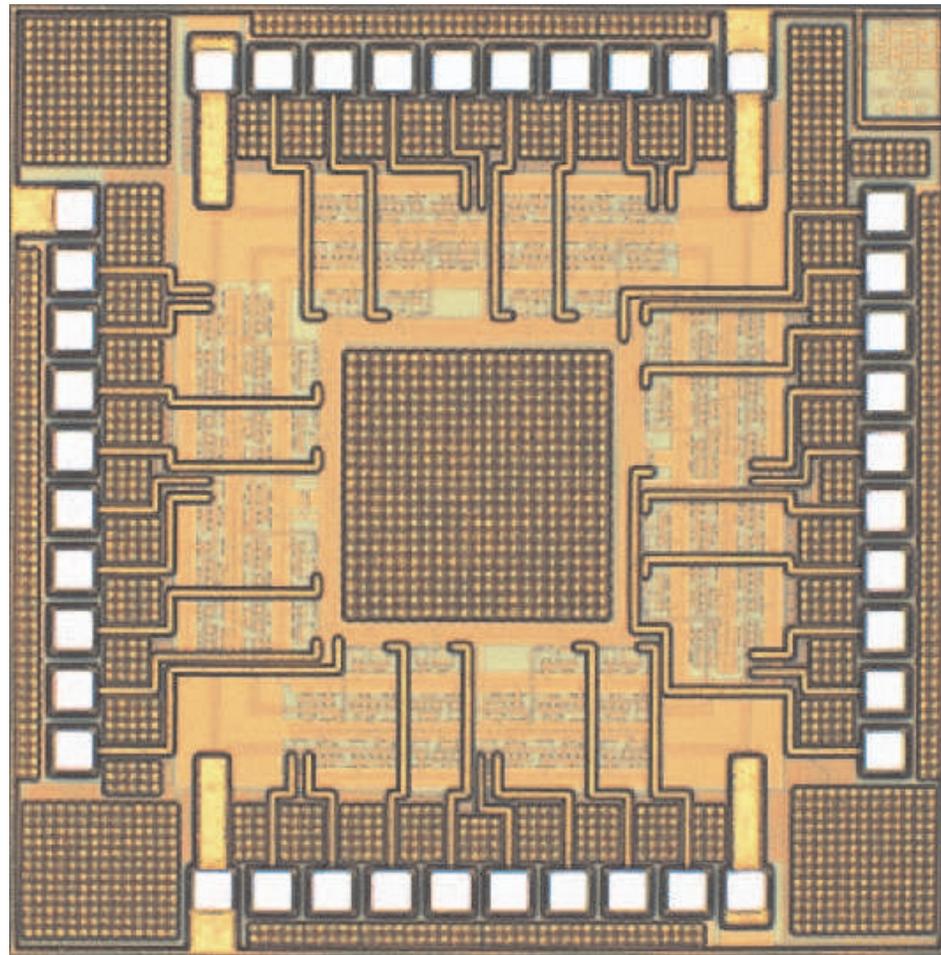
Building a Turbo code from memory two tailbiting convolutional code

Simulation measurement results

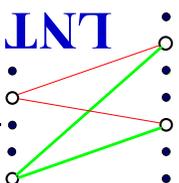


The analog decoder outperforms 6 digital iterations





High Speed Implementation of the (16,8,3) Tailbiting Code (2001) by TUM/Lucent



Comparison of Several Implementations

	TUM	ETH	University of Utah	Universities of Padova, Torino
code	(16,8,3), m=1	(18,9,5), m=2	(8,4,4) ext. Hamming	UMTS, 1/3, mem. 3
process	0.25 μ m BiCMOS	IBM6HP	0.8 μ m BiCMOS	0.35 μ m CMOS
chip area	1.68mm ²	1.64mm ²	7.28mm ²	2.25mm ²
transistor	441	940	-	-
# bipolar	356	-	n.a.	n.a.
# nMOS	-	650	n.a.	n.a.
# pMOS	-	44.17	n.a.	n.a.
total # per inf.bit&state	49.8	54.4	n.a.	n.a.
supply	3.3V	3.3V	5V	3.3 V
bias	80 μ A (nMOS)	400 μ A	200 μ A or 50 μ A	10 μ A
per block	20mW	150mW	98mW @ 200 μ A	5.6mW
power consumption			50mW @ 50 μ A	
power per inf.bit&state	1.25mW	9.4mW	2.72mW @ 200 μ A 1.38mW @ 50 μ A	0.32mW
measurements				
channel	AWGN	AWGN	BSC	AWGN
speed	160Mbit/s	10 Gbit/s	100Mbit/s	10Mbit/s
BER	yes	tbd.	n.a.	n.a.
year chip worked?	1999 Yes	2002 Yes	2001 ?	2001
				2003 ?

Conclusions

- The **Turbo Principle** is a very general principle
- Approaching the capacity limits of mobile systems is possible
- Analog FEC Decoders are possible and have many advantages especially for **tailbiting convolutional codes (TBCC) and turbo decoding**
- Proof of concept prototype analog VLSI of TUM/Lucent with TBCC works at up to **10 Gbit/s**.
- Worldwide nine groups currently working on analog decoder design
- There are many more applications for the **Turbo Principle**:
 - Turbo source compression
 - Joint source channel coding
 - Interference cancellation

Papers can be downloaded from WWW.LNT.EI.TUM.DE